REMARKS

The Final Office Action dated June 8, 2005 has been received and carefully considered. In this response, claims 38 and 44-49 have been amended to provide grammatical consistency. The amendments to the claims do not narrow the scope of the claims. Reconsideration of the outstanding rejection in the present application is respectfully requested based on the following remarks.

Obviousness Rejection of Claims 38-49

At paragraph 5 of the Final Office Action, claims 38-49 were rejected under 35 U.S.C. Section 102(b) as being anticipated by Lee (U.S. Patent No. 4,763,242). This rejection is respectfully traversed.

Claim 38, from which claims 39-43 depend, recites the features of a method for a processor to initiate, via a coprocessor bus, execution by a coprocessor of an instruction received by the processor for execution thereby, the method comprising receiving said instruction, decoding said instruction, and providing to said coprocessor, *at least partially coincident with said decoding*, at least a predetermined portion of said instruction via a first portion of said coprocessor bus and a first control signal indicating that said instruction is being decoded by said processor via a second portion of said coprocessor bus.

As discussed in the response to the previous Office Action, Lee fails to disclose that at least a predetermined portion of an instruction and a first control signal are provided to a coprocessor via a coprocessor bus at least partially coincident with the decoding of the instruction. *See Previous Response*, p. 9. At paragraph 7, the Final Office Action asserts "[t]he terminology argue [sic] does not appear in the specification, *applicant is required to provide the relevant portion of the specification to which the definition 'at least partially coincident with said decoding', he is alleging is not taught*" (emphasis added). The Applicant notes that none of the claims are rejected under 35 U.S.C. Section 112, first paragraph. Moreover, as stated in MPEP Section 2163.02, the fundamental factual inquiry for enablement is whether a claim defines an invention that is clearly conveyed to those skilled in the art at the time the application

was filed. The subject matter of the claim need not be described literally (i.e., using the same terms or in *haec verba*) in order for the disclosure to satisfy the description requirement. Accordingly, the Final Office Action errs in requiring that the Applicant particularly describe how the specification defines "at least partially coincident with said decoding" based on a rejection under 35 U.S.C. Section 102(b). Nevertheless, in an effort to advance the present application to issuance and to assist the Office, the Applicant notes that Figure 5 and its related disclosure describe an illustrative embodiment of providing a portion of an instruction at least partially coincident with the decoding of the instruction. As exemplary illustrated by Figure 5, an instruction decode strobe H_DEC* signal 63 "is provided to indicate the decode of an coprocessor interface opcode by the processor 12" and the instruction bus H_OP[11:0] 61 "provides the coprocessor interface 30 opcode being issued to the external coprocessor 14" *Present Application*, p. 11, lines 9-11 and p. 10, lines 14-16. As Figure 5 illustrates, the H_DEC* signal 63 is asserted after the first rising edge of the clock signal 60, thereby indicating that the opcode XX (one embodiment of an instruction) is being decoded (see top of Figure 5 "DECODE H_OP XX, NOT BUSY"), and at least a portion of the transmission of the opcode XX via H_OP[11:0] bus 61 occurs while the H_DEC* signal 63 is asserted (i.e., at least partially coincident with the decoding of the opcode XX). Thus, in view of the illustrative embodiment of Figure 5, *inter alia*, the specification provides sufficient support for the recited claim language "at least partially coincident with said decoding."

At paragraph 5, the Final Office Action asserts that the claimed features of providing to said coprocessor, *at least partially coincident with said decoding*, at least a predetermined portion of said instruction via a first portion of said coprocessor bus are disclosed by the passages of Lee at col. 2, lines 57-63 and col. 4, lines 48-68. For ease of reference, these cited passages of Lee are reproduced in their entirety below:

> An SFU receives and sends data to the main processor's registers. An SFU can be incorporated into the computer by directly impacting internal register buses of the main processor. Direct coupling to the main processor's internal register buses enables an SFU to achieve a very high performance level.

Lee, col. 2, lines 57-63.

> Instruction 127 comprises a processor field 129 and an assist field 131. Control unit 115 decodes processor field 129. If processor field 129 indicates that instruction 127 is a basic instruction, processor functional unit 117 executes instruction 127, loading or storing any required operands or results in plurality of registers 119 or in memory system 111.
>
> If processor field 129 indicates that instruction 127 is an assist instruction, stores a copy of instruction 127 is stored in a register among plurality of registers 119. An instruction space and an instruction offset which indicate a memory address 161 at which instruction 127 is located are also stored in registers 119. If a data reference is specified in instruction 127, a data space and a data offset which indicate a data address are also stored in registers 119.

Id., col. 4, lines 48-68.

The relied-upon passages of Lee disclose merely the transfer of an instruction 127 to either SFU or COP 109 when the instruction 127 is an assist instruction. These passages do not disclose or suggest that this transfer is at least partially coincident with the decoding of the instruction 127. Accordingly, neither of these passages, nor any other passage of Lee, discloses or suggests providing at least a predetermined portion of an instruction to a coprocessor via a first portion of a coprocessor at least partially coincident with the decoding of the instruction by the processor as provided by claim 38.

Claim 38 further recites the features of providing to said coprocessor, *at least partially coincident with said decoding*, a first control signal indicating that said instruction is being decoded by said processor via a second portion of said coprocessor bus. At paragraph 5, the Final Office Action asserts that these features are disclosed by the passage of Lee at col. 8, lines 3-8. For ease of reference, this cited passage is reproduced in its entirety below:

> AINIT 602 is a signal from main processor 103 for timing and identifying "assist cycles." ADTR 604 is a signal from main processor 103 for identifying whether an assist cycle is a data transfer cycle or a command cycle. ARDY 612 is a response signal from an assist for indicating that the assist is ready to continue.

Lee, col. 8, lines 3-8.

Lee does not disclose or suggest that any of the signals AINIT 602, ADTR 604, or ARDY 612 indicate in any manner that an instruction is being decoded by a processor, nor that any of these signals are provided to a coprocessor at least partially coincident with the decoding

of the instruction by the processor. It therefore is submitted that Lee fails to disclose or suggest the features of providing to said coprocessor, *at least partially coincident with said decoding*, a first control signal indicating that said instruction is being decoded by said processor via a second portion of said coprocessor bus as recited by claim 38.

As discussed above, Lee fails to disclose or suggest at least the features of providing to said coprocessor, *at least partially coincident with said decoding*, at least a predetermined portion of said instruction via a first portion of said coprocessor bus and a first control signal indicating that said instruction is being decoded by said processor via a second portion of said coprocessor bus as recited by claim 38. Accordingly, the Office Action fails to establish that Lee discloses or suggests each and every feature of claim 38, as well as each and every feature of claims 39-43 at least by virtue of their dependency from claim 38. Moreover, claims 39-43 recite additional features neither disclosed nor suggested by Lee.

Claim 44 recites the features of receiving from a processor a first control signal indicating that an instruction *is being decoded* via a second portion of a coprocessor bus. At paragraph 5, the Final Office Action asserts that claim 44 fails to "teach or define above or beyond claims 38-44, and are rejected for the reasons set forth supra." None of the passages of Lee cited by the Final Office Action, or any other passage of Lee, discloses or suggests providing a signal to a coprocessor to indicate that an instruction *is being* decoded. Lee therefore fails to disclose or suggest the features of receiving from a first processor a first control signal indicating that an instruction is being decoded via a second portion of a coprocessor bus as recited by claim 44. Accordingly, the Final Office Action fails to establish that Lee discloses or suggests each and every feature recited by claim 44, as well as each and every feature recited by claim 45 at least by virtue of its dependency from claim 44. Moreover, claim 45 recites additional features neither disclosed nor suggested by Lee.

To illustrate, claim 44 recites the feature of providing to said processor a second control signal indicating said instruction caused an exception and claim 45 recites the additional features of wherein said second control signal is provided to said processor prior to said instruction completing in said processor. None of the cited passages nor any other passage of Lee discloses

or suggests that a control signal indicating that an instruction caused an exception is provided to a processor prior to the instruction completing in the processor.

Claim 46 recites the features of, in a processor, decoding an instruction and providing to a coprocessor, *at least partially coincident with said decoding*, at least a predetermined portion of said instruction via a first portion of said coprocessor bus and a first control signal indicating that said instruction is being decoded by said processor via a second portion of said coprocessor bus. Claims 47 and 49 also recite these features. As discussed above with respect to claim 38, Lee fails to disclose or suggest providing at least a predetermined portion of an instruction and a control signal indicating that the instruction is being decoded by a processor to a coprocessor at least partially coincident with the decoding of the instruction. Accordingly, it is respectfully submitted that the Office Action fails to establish that Lee discloses or suggests each and every feature of claims 46, 47 and 49.

Claim 48 recites the features of receiving from a processor a first control signal indicating that an instruction *is being decoded* by said processor via a second portion of a coprocessor bus. As noted above with respect to claim 44, Lee fails to disclose or suggest providing a signal from a processor to a coprocessor indicating that an instruction *is being decoded* by the processor. Accordingly, it is respectfully submitted that the Office Action fails to establish that Lee discloses or suggests each and every feature of claim 48.

In view of the foregoing, it is respectfully submitted that the anticipation rejection of claims 38-49 is improper at this time and the withdrawal of this rejection therefore is respectfully requested.

Conclusion

The Applicant respectfully submits that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

The Commissioner is hereby authorized to charge any fees that may be required, or credit any overpayment, to Deposit Account Number 50-2469.

Respectfully submitted,

5 August 2005
Date

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